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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/650,726	08/30/2000	Denis Miglianico	Q60462	1213

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EXAMINER	
DAY, HERNG DER	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 08/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/650,726	MIGLIANICO, DENIS	
	Examiner	Art Unit	
	Herng-der Day	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to Applicant's Amendment ("Amendment") to Office Action dated February 4, 2005, mailed June 6, 2005.

1-1. Claim 7 has been amended. Claim 11 has been cancelled. Claims 1-3 and 5-10 are pending.

1-2. Claims 1-3 and 5-10 have been examined and rejected.

Specification

2. The objection to the specification has been withdrawn.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 5-7, and 9-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Hanselmann, "Real-Time Simulation Replaces Test Drives", Test and Measurement World, February 15, 1996, pages 35-36, 38, 40.

4-1. Regarding claim 1, Hanselmann discloses a method of testing the operation of an electronic unit (electronic control unit, page 35, FIGURE 1) by stimulating said unit with simulated input signals to said unit, the method comprising:

processing at least one output signal from said unit at a first frequency in response to said simulated input signals (Torque Command or Pressure Sensors output, page 35, FIGURE 1);

storing values of parameters corresponding to said processed signals (records time histories on the DSP, page 38, center column, last paragraph); and

accessing said stored parameter values (upload them to the MATLAB workspace, page 38, center column, last paragraph) at a second frequency which is slower than said first frequency and is compatible with an operating frequency of a microprocessor that generates said simulated input signals (DSP generate signals much faster than the vehicle simulation, page 36, right column, paragraph 3).

4-2. Regarding claim 2, Hanselmann further discloses said parameter values are representative of switching instants of logic signals generated by said unit (Torque Command, page 35, FIGURE 1).

4-3. Regarding claim 3, Hanselmann further discloses said parameter values are an image of said switching instants, of the duration during which a logic variable has a predetermined value, and/or the mean value of a logic variable over a predetermined period (postprocessing, page 38, right column, paragraph 2).

4-4. Regarding claim 5, Hanselmann discloses an apparatus for testing the operation of an electronic unit (electronic control unit, page 35, FIGURE 1) by simulation, said unit generating logic signals at specific instants, said apparatus comprising:

a simulator (Simulator, page 35, FIGURE 1) which comprises at least one microprocessor (for example, Master DSP, page 35, FIGURE 1) sending input simulation signals to said unit (electronic control unit, page 35, FIGURE 1) and receiving output signals from said unit in

response to said input simulation signals (for example, one of the Parallel Processing DSP, page 35, FIGURE 1);

at least one programmable logic circuit (for example, one of the Parallel Processing DSP, page 35, FIGURE 1) which receives at least one of said output signals, said logic circuit generating, at a first frequency, parameter values corresponding to the signals received by said logic circuit (DSP generate signals much faster than the vehicle simulation, page 36, right column, paragraph 3); and

a storing circuit which stores said parameter values (records time histories on the DSP, page 38, center column, last paragraph), wherein said microprocessor accesses said stored parameter values at a second frequency which slower than said first frequency and is compatible with an operating frequency of said microprocessor (upload them to the MATLAB workspace, page 38, center column, last paragraph).

4-5. Regarding claim 6, Hanselmann further discloses comprising at least one second programmable logic circuit which sends in real time simulation signals to said unit on the basis of reference signals previously issued by said microprocessor (DDS board contains its own DSPs, page 36, right column, paragraph 3).

4-6. Regarding claim 7, Hanselmann further discloses said programmable logic circuit which receives said some of said output signals and said second programmable logic circuit which sends simulation signals to said unit are implemented as a single electronic circuit (DDS board, page 36, right column, paragraph 3).

4-7. Regarding claim 9, Hanselmann further discloses said simulator further comprises at least one of:

an analog-to-digital converter which forward digital signals representative of analog signals generated by said unit to said microprocessor, and a digital-to-analog converter which forwards analog simulation signals based on digital signals generated by said microprocessor to said unit (digital-to-analog converter, page 36, right column, paragraph 2).

4-8. Regarding claim 10, Hanselmann further discloses at least one of said programmable logic circuit and said second programmable logic circuit is programmed as a function of the type and/or intended use of said unit (Generating wheel-speed signal, page 36, right column, paragraph 4).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hanselmann, "Real-Time Simulation Replaces Test Drives", Test and Measurement World, February 15, 1996, pages 35-36, 38, 40, in view of Turner, U.S. Patent 6,269,020 B1 issued July 31, 2001, and filed February 5, 1999.

6-1. Regarding claim 8, Hanselmann fails to disclose at least one of said programmable logic circuit and said second programmable logic circuit is of the field programmable gate array type.

Turner discloses, as shown in FIG. 1, a processing unit incorporates a programmable logic device and the processing unit may be a DSP (column 1, lines 40-60). Turner further

discloses, "Programmable logic devices (sometimes referred to as a PALs, PLAs, FPLAs, PLDs, EPLDs, EEPLDs, LCAs, or FPGA), are well-known integrated circuits that provide the advantages of fixed integrated circuits with the flexibility of custom integrated circuits. Such devices allow a user to electrically program standard, off-the-shelf logic elements to meet a user's specific needs" (column 1, lines 22-28).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Hanselmann to incorporate the teachings of Turner to obtain the invention as specified in claim 8 because FPGA is well-known and allows a user to electrically program standard, off-the-shelf logic elements to meet a user's specific needs.

Applicant's Arguments

7. Applicant argues the following:

(1) "Applicant herein cancels claim 11 without prejudice and/or disclaimer" (page 7, the last second paragraph, Amendment).

(2) "Applicant herein amends claim 7 to recite 'said at least one of said output signals' instead of 'said some of said output signals'" (page 7, the last paragraph, Amendment).

(3) "All that Hanselmann et al. disclose is that the DDS DSPS generate input signals for the unit under test at a rate that is faster than the vehicle simulation executing in the master DSP. There is no teaching or suggestion that the DDS DSPS generate parameter values, based on output signals received from the unit under test, at a frequency that is greater than an accessing frequency" (page 9, paragraph 1, Amendment).

(4) "there is no teaching or suggestion that the DDS DSPS receive output signals from the unit under test in response to an input signal" (page 10, paragraph 1, Amendment).

(5) "Applicant submits that claim 1 is allowable for at least reasons analogous to those discussed above with respect to claim 5" (page 11, paragraph 1, Amendment).

(6) "Applicant submits that claim 8 is patentable at least by virtue of its dependency from claim 5" (page 11, the last paragraph, Amendment).

Response to Arguments

8. Applicant's arguments have been fully considered.

8-1. Applicant's argument (1) is persuasive. The rejection of claim 11 under 35 U.S.C. 112, first paragraph, in the Office Action dated February 4, 2005, has been withdrawn.

8-2. Applicant's argument (2) is persuasive. The rejection of claim 7 under 35 U.S.C. 112, second paragraph, in the Office Action dated February 4, 2005, has been withdrawn.

8-3. Applicant's arguments (3) - (6) are not persuasive. First, as described at page 36, column 1, paragraph 1, Hanselmann et al. disclose, "The gray box on the left contains the real-time hardware for the test bench - multiple digital signal processors (DSPs), I/O boards, and interfacing circuitry" and "The real-time hardware handles all closed-loop computing, which has to meet stringent time requirements". Accordingly, at least one of the multiple DSPs (programmable logic circuits) has to receive at least one of the output signals from the unit under test and generate parameter values corresponding to the received signals in order to meet the requirement - "the real-time hardware handles all closed-loop computing". Second, as described at page 36, column 3, paragraph 3, Hanselmann et al. disclose the DSP generates signals much

faster than the vehicle simulation. In other words, the DSP receives the output signals and generate parameter values at a frequency that is greater than an accessing frequency. Therefore, storing the generated parameter values and waiting for the processing by the Master DSP is necessary.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Herng-der Day whose telephone number is (571) 272-3777. The Examiner can normally be reached on 9:00 - 17:30.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: (571) 272-2100.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Jean R. Homere can be reached on (571) 272-3780. The fax phone numbers for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Herng-der Day
August 22, 2005 H.D.

Thai Phan
Patent Examiner
AU: 2128